MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016 SESSION

ECE3226- ADVANCED COMPUTER ARCHITECTURE AND PARALLEL COMPUTING

(CE)

02 MARCH 2016
02:30 P.M – 04:30 P.M
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of five (5) pages only (including this page).
2. There are **FOUR (4) QUESTIONS** in this paper. Answer **ALL QUESTIONS**. All questions carry 25 marks each.
3. Write your answers in the Answer Booklet provided.

Question 1

a) In your own words, give a description on the Flynn's classification of Computer Architecture. [4 marks]

b) With the help of diagrams, illustrate the differences in characteristics of SIMD and MIMD computer architecture with diagrams. [8 marks]

c) P1 and P2 are two implementations of the same instruction set. A, B, C, D and E are the five classes of instructions which are available in the instruction set. P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is shown in Table 1:

Table 1

Class	CPI on P1	CPI on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	3	4

i) Estimate the peak performances of P1 and P2 in terms of instructions per second by assuming that the peak performance as the fastest rate that a computer can execute any instruction sequence. [4 marks]

ii) Assuming the number of instructions executed in the sample program consists of equally divided classes A, B, C, D and E, and class A appearing twice in the program, calculate how much faster P2 is than P1? [5 marks]

d) An enhancement to a computer is made such that it improves certain mode of execution by a factor of 10. An enhanced mode is used 50% of the time, measured as a percentage of the execution time when the enhanced mode is in use. Recall that Amdahl's law depends on the fraction of the original, unenhanced execution time that could make use of enhanced mode. Thus, we cannot directly use this 50% measurement to compute speedup with Amdahl's law.

i) Calculate and determine the speedup we have obtained from fast mode? [2 marks]

ii) Find the percentage of the original execution time which has been converted to fast mode? [2 marks]

Continued...

Question 2

a) A DLX processor is designed based on RISC architecture initiated by John L. Hennessy and David A. Patterson.

i) State the four classes of instruction of a DLX processor and explain them in your own words. [4 marks]

ii) List down the five phases of DLX operation. [5 marks]

b) A pipeline helps in the throughput of the entire workload but it does not improve the latency on each individual process. Assume a five stage single-pipeline microarchitecture (fetch, decode, execute, memory, write-back) and the code below

```
Loop:  LW     R3,0(R0)
       LW     R1,0(R3)
       ADDI   R1,R1,#1
       SUB    R4,R3,R2
       SW     R1,0(R3)
       BNZ    R4, Loop
```

All ops are one cycle except LW and SW, which are 1+2 cycles, and branches, which are 1+1 cycles. There is no forwarding.

i) Show and briefly explain the phases of each instruction per clock cycle for one iteration of the loop [4 marks]

ii) Calculate the number of clock cycles per loop iteration which is lost to branch overhead. [2 marks]

iii) Assume there is a static branch predictor, capable of recognizing a backward branch in the Decode stage. Estimate the number of clock cycles that are wasted on branch overhead. [2 marks]

iv) Assuming with a dynamic branch predictor, calculate the number of cycles are lost on a correct prediction? [2 marks]

c) State the hazards that prevent next instruction from executing during its designated clock cycle. [6 marks]

Continued...

Question 3

a) Define and elaborate the following terms: vector, vector processing and vectorizer. [6 marks]

b) State and explain briefly the properties of vector processing. [8 marks]

c) Show the following code sequence lay out in convoys by assuming there is a single copy of each vector functional unit:

```
LV      V1,Rx      ;load vector X
MULVS.D V2,V1,F0   ;vector-scalar multiply
LV      V3,Ry      ;load vector Y
ADDVV.D V4,V2,V3   ;add two vectors
SV      V4,Ry      ;store the sum
```

[4 marks]

i) Estimate the number of chimes that could be taken by this vector sequence. [1 mark]

ii) By ignoring the vector instruction issue overhead, estimate the required number of cycles per FLOP (floating-point operation). [2 marks]

d) There are 8 memory banks provided in the system, with a bank busy time of 6 clocks and a total memory latency of 12 cycles.

i) Calculate the time taken to complete a 64 elements vector load with a stride of 1. [2 marks]

ii) Calculate the time taken to complete a 64 elements vector load with a stride of 32. [2 marks]

Continued...

Question 4

a) List down the FOUR performance parameters of interconnection network and explain each of them in your own words. [8 marks]

b) State the FIVE major structures of MIT computer architecture and briefly explain them. [5 marks]

c) Derive and sketch a data-flow graph for the if-else statement shown in figure Q4c.

```
if (i> 20 )
{
        j = ( i + 4 ) * 2;
}
else
{
        j = ( i – 2 ) * 2 ;
}
```

Figure: Q4c

[6 marks]

e) Show and draft the data flow graph to evaluate the expression.

$$Y = 1 + \frac{X^2}{2} + \frac{X^4}{4} + \frac{X^6}{6}$$

[6 marks]

End of Paper